DATA SHEET

74LVCH322244A

32-bit buffer/line driver; with 30 Ω series termination resistors; 5 V input/output tolerant; 3-state

Product specification
Supersedes data of 1999 Aug 31

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FEATURES

- 5 V tolerant inputs/outputs for interfacing with 5 V logic
- Wide supply voltage range from 1.2 V to 3.6 V
- CMOS low power consumption
- MULTIBYTE flow-trough standard pin-out architecture
- Low inductance multiple power and ground pins for minimum noise and ground bounce
- Direct interface with TTL levels
- Inputs accept voltages up to 5.5 V
- All data inputs have bushold
- Integrated 30 Ω termination resistors
- Complies with JEDEC standard JESD8B/JESD36
- ESD protection:
  HBM EIA/JESD22-A114-B exceeds 2000 V
  MM EIA/JESD22-A115-A exceeds 200 V.
- Specified from –40 °C to +85 °C
- Packaged in plastic fine-pitch ball grid array package.

DESCRIPTION

The 74LVCH322244A is a high-performance, low-power, low-voltage, Si-gate CMOS device, superior to most advanced CMOS compatible TTL families. Inputs can be driven from either 3.3 V or 5 V devices. In 3-state operation, outputs can handle 5 V. These features allow the use of these devices in a mixed 3.3 V and 5 V environment.

The 74LVCH322244A is a 32-bit non-inverting buffer/line driver with 3-state outputs. The 3-state outputs are controlled by the output enable inputs n$\overline{OE}$. A HIGH on input n$\overline{OE}$ causes the outputs to assume a high-impedance OFF-state.

The 74LVCH322244A is designed with 30 Ω series termination resistors in both HIGH and LOW output stages to reduce line noise.

To ensure the high-impedance state during power-up or power-down, input n$\overline{OE}$ should be tied to V_{CC} through a pull-up resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The 74LVCH322244A bushold data input circuit eliminates the need for external pull-up resistors to hold unused or floating data inputs at a valid logic level.

QUICK REFERENCE DATA

Ground = 0 V; T_{amb} = 25 °C; $t_r = t_f \leq 2.5$ ns.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay nAn to nYn	C_L = 50 pF; V_{CC} = 3.3 V	3.0	ns
t_{PZH}/t_{PZL}	3-state output enable time n$\overline{OE}$ to nYn	C_L = 50 pF; V_{CC} = 3.3 V	3.5	ns
t_{PHZ}/t_{PLZ}	3-state output disable time n$\overline{OE}$ to nYn	C_L = 50 pF; V_{CC} = 3.3 V	2.8	ns
C_I	input capacitance		5.0	pF
C_{PD}	power dissipation capacitance per gate	V_I = 3.3 V; notes 1 and 2		
		outputs enabled	12	pF
		outputs disabled	4.0	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
   $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz;
   f_o = output frequency in MHz;
   C_L = output load capacitance in pF;
   V_{CC} = supply voltage in Volts;
   N = total load switching outputs;
   $\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}.

FUNCTION TABLE

See note 1.

INPUT		OUTPUT
$n\overline{OE}$	nAn	nYn
L	L	L
L	H	H
H	X	Z

Note

1. H = HIGH voltage level;
   L = LOW voltage level;
   X = don't care;
   Z = high-impedance OFF-state.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE				
	TEMPERATURE RANGE	BALLS	PACKAGE	MATERIAL	CODE
74LVCH322244AEC	–40 °C to +85 °C	96	LFBGA96	plastic	SOT536-1

PINNING

BALL	SYMBOL	DESCRIPTION
A1	1Y1	data output
A2	1Y0	data output
A3	$1\overline{OE}$	3-state output enable inputs (active LOW)
A4	$2\overline{OE}$	3-state output enable inputs (active LOW)
A5	1A0	data input
A6	1A1	data input
B1	1Y3	data output
B2	1Y2	data output
B3, B4, D3, D4, E3, E4, G3, G4, K3, K4, M3, M4, N3, N4, R3, R4	GND	ground (0 V)
B5	1A2	data input
B6	1A3	data input
C1	2Y1	data output
C2	2Y0	data output

BALL	SYMBOL	DESCRIPTION
C3, C4, F3, F4, L3, L4, P3, P4	V_{CC}	supply voltage
C5	2A0	data input
C6	2A1	data input
D1	2Y3	data output
D2	2Y2	data output
D5	2A2	data input
D6	2A3	data input
E1	3Y1	data output
E2	3Y0	data output
E5	3A0	data input
E6	3A1	data input
F1	3Y3	data output
F2	3Y2	data output
F5	3A2	data input
F6	3A3	data input
G1	4Y1	data output
G2	4Y0	data output
G5	4A0	data input
G6	4A1	data input

BALL	SYMBOL	DESCRIPTION
H1	4Y2	data output
H2	4Y3	data output
H3	$4\overline{OE}$	3-state output enable inputs (active LOW)
H4	$3\overline{OE}$	3-state output enable inputs (active LOW)
H5	4A3	data input
H6	4A2	data input
J1	5Y1	data output
J2	5Y0	data output
J3	$5\overline{OE}$	3-state output enable inputs (active LOW)
J4	$6\overline{OE}$	3-state output enable inputs (active LOW)
J5	5A0	data input
J6	5A1	data input
K1	5Y3	data output
K2	5Y2	data output
K5	5A2	data input
K6	5A3	data input
L1	6Y1	data output
L2	6Y0	data output
L5	6A0	data input
L6	6A1	data input
M1	6Y3	data output

BALL	SYMBOL	DESCRIPTION
M2	6Y2	data output
M5	6A2	data input
M6	6A3	data input
N1	7Y1	data output
N2	7Y0	data output
N5	7A0	data input
N6	7A1	data input
P1	7Y3	data output
P2	7Y2	data output
P5	7A2	data input
P6	7A3	data input
R5	8A0	data input
R6	8A1	data input
R1	8Y1	data output
R2	8Y0	data output
T1	8Y2	data output
T2	8Y3	data output
T3	$8\overline{OE}$	3-state output enable inputs (active LOW)
T4	$7\overline{OE}$	3-state output enable inputs (active LOW)
T5	8A3	data input
T6	8A2	data input

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	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T
6	1A1	1A3	2A1	2A3	3A1	3A3	4A1	4A2	5A1	5A3	6A1	6A3	7A1	7A3	8A1	8A2
5	1A0	1A2	2A0	2A2	3A0	3A2	4A0	4A3	5A0	5A2	6A0	6A2	7A0	7A2	8A0	8A3
4	$2\overline{OE}$	GND	V_{CC}	GND	GND	V_{CC}	GND	$3\overline{OE}$	$6\overline{OE}$	GND	V_{CC}	GND	GND	V_{CC}	GND	$7\overline{OE}$
3	$1\overline{OE}$	GND	V_{CC}	GND	GND	V_{CC}	GND	$4\overline{OE}$	$5\overline{OE}$	GND	V_{CC}	GND	GND	V_{CC}	GND	$8\overline{OE}$
2	1Y0	1Y2	2Y0	2Y2	3Y0	3Y2	4Y0	4Y3	5Y0	5Y2	6Y0	6Y2	7Y0	7Y2	8Y0	8Y3
1	1Y1	1Y3	2Y1	2Y3	3Y1	3Y3	4Y1	4Y2	5Y1	5Y3	6Y1	6Y3	7Y1	7Y3	8Y1	8Y2

Fig.1 Pin configuration.

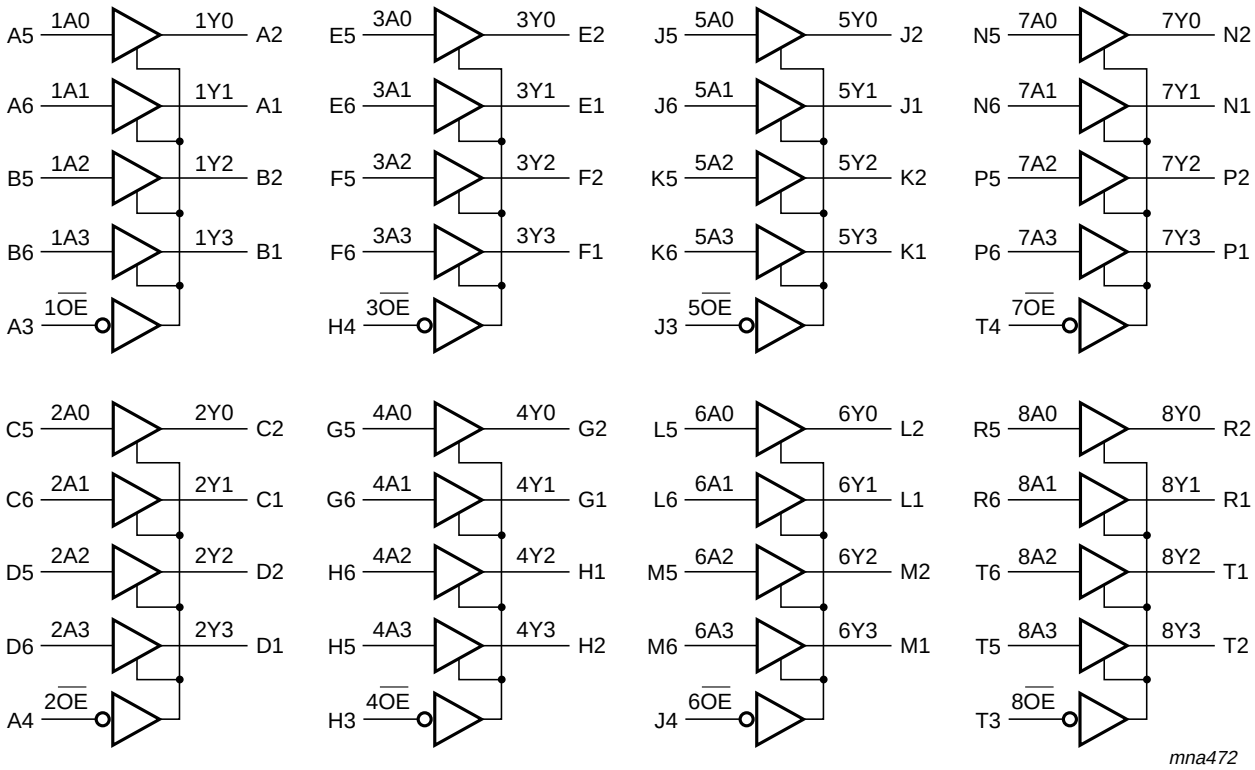


Fig.2 Logic symbol.

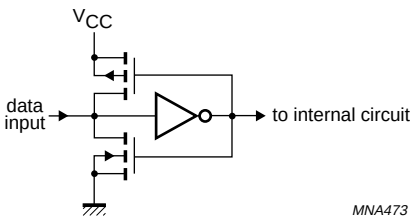


Fig.3 Bushold circuit.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	supply voltage	for maximum speed performance	2.7	3.6	V
		for low-voltage applications	1.2	3.6	V
V_I	input voltage		0	5.5	V
V_O	output voltage	output HIGH or LOW state	0	V_{CC}	V
		3-state	0	5.5	V
T_{amb}	operating ambient temperature	see DC and AC characteristics per device	–40	+85	°C
t_r, t_f ($\Delta t/\Delta f$)	input rise and fall times ratio	V_{CC} = 1.2 V to 2.7 V	0	20	ns/V
		V_{CC} = 2.7 V to 3.6 V	0	10	ns/V

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134); voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	supply voltage		–0.5	+6.5	V
V_I	input voltage	note 1	–0.5	+6.5	V
I_{IK}	input diode current	V_I < 0 V	–	–50	mA
I_{OK}	output diode current	V_O > V_{CC} or V_O < 0 V; note 1	–	±50	mA
V_O	output voltage	output HIGH or LOW state; note 1	–0.5	V_{CC} + 0.5	V
		output 3-state; note 1	–0.5	+6.5	V
I_O	output source or sink current	V_O = 0 V to V_{CC}	–	±50	mA
I_{CC}, I_{GND}	V_{CC} or GND current		–	±200	mA
T_{stg}	storage temperature		–65	+150	°C
P_{tot}	power dissipation per packages	temperature range: T_{amb} = –40 °C to +85 °C; note 2	–	1000	mW

Notes

1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. Above 70 °C the value of P_{tot} derates linearly with 1.8 mW/K.

DC CHARACTERISTICS

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		OTHER	V_{CC} (V)				
T_{amb} = –40 °C to +85 °C; note 1							
V_{IH}	HIGH-level input voltage		1.2	V_{CC}	–	–	V
			2.7 to 3.6	2.0	–	–	V
V_{IL}	LOW-level input voltage		1.2	–	–	GND	V
			2.7 to 3.6	–	–	0.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}					
		I_O = –100 μA	2.7 to 3.6	V_{CC} – 0.2	V_{CC}[2]	–	V
		I_O = –6 mA	2.7	V_{CC} – 0.5	–	–	V
		I_O = –12 mA	3.0	V_{CC} – 0.8	–	–	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}					
		I_O = 100 μA	2.7 to 3.6	–	GND[2]	0.20	V
		I_O = 6 mA	2.7	–	–	0.40	V
		I_O = 12 mA	3.0	–	–	0.55	V
I_{LI}	input leakage current	V_I = 5.5 V or GND; note 3	3.6	–	±0.1	±5	μA
I_{OZ}	3-state output OFF-state current	V_I = V_{IH} or V_{IL}; V_O = 5.5 V or GND	3.6	–	±0.1	±5	μA
I_{off}	power-off leakage supply current	V_I or V_O = 5.5 V	0.0	–	±0.1	±10	μA
I_{CC}	quiescent supply current	V_I = V_{CC} or GND; I_O = 0 A	3.6	–	0.1	40	μA
ΔI_{CC}	additional quiescent supply current	V_I = V_{CC} – 0.6 V; I_O = 0 A; per input pin	2.7 to 3.6	–	5[2]	500	μA
I_{BHL}	bushold LOW sustaining current	V_I = 0.8 V; notes 4 and 5	3.0	75	–	–	μA
I_{BHH}	bushold HIGH sustaining current	V_I = 2.0 V; notes 4 and 5	3.0	–75	–	–	μA
I_{BHLO}	bushold LOW overdrive current	notes 4 and 6	3.6	500	–	–	μA
I_{BHHO}	bushold HIGH overdrive current	notes 4 and 6	3.6	–500	–	–	μA

Notes

1. All typical values are measured at T_{amb} = 25 °C.
2. Value is measured at V_{CC} = 3.3 V.
3. For bushold parts the bushold circuit is switched off when V_I exceeds V_{CC} allowing 5.5 V on the input terminal.
4. For data inputs only. Control inputs do not have a bushold circuit.
5. The specified sustaining current at the data input holds the input below the specified V_I level.
6. The specified overdrive current at the data input forces the data input to the opposite logic input level.

AC CHARACTERISTICS

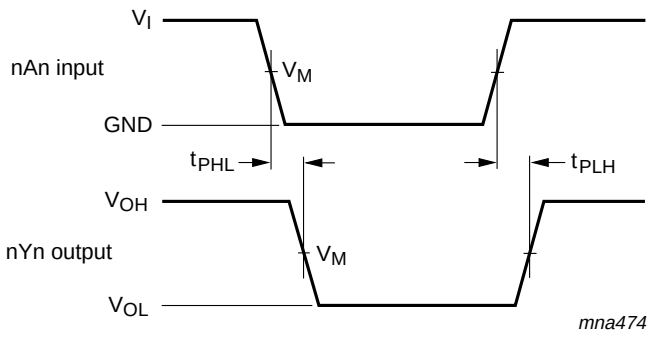
Ground = 0 V; $t_r = t_f \leq 2.5$ ns; $C_L = 50$ pF; $R_L = 500\ \Omega$.

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		WAVEFORMS	V_{CC} (V)				
T_{amb} = −40 to +85 °C; note 1							
t_{PHL}/t_{PLH}	propagation delay nAn to nYn	see Figs 4 and 6	1.2	–	11.0	–	ns
			2.7	1.0	–	6.7	ns
			3.0 to 3.6	1.0	3.0(2)	5.8	ns
t_{PZH}/t_{PZL}	3-state output enable time $n\overline{OE}$ to nYn	see Figs 5 and 6	1.2	–	15.0	–	ns
			2.7	1.5	–	7.6	ns
			3.0 to 3.6	1.0	3.5(2)	6.0	ns
t_{PHZ}/t_{PLZ}	3-state output disable time $n\overline{OE}$ to nYn	see Figs 5 and 6	1.2	–	10.0	–	ns
			2.7	1.5	–	4.7	ns
			3.0 to 3.6	1.5	2.8(2)	4.5	ns
$t_{sk(0)}$	skew		3.0 to 3.6	–	–	1.0	ns

Notes

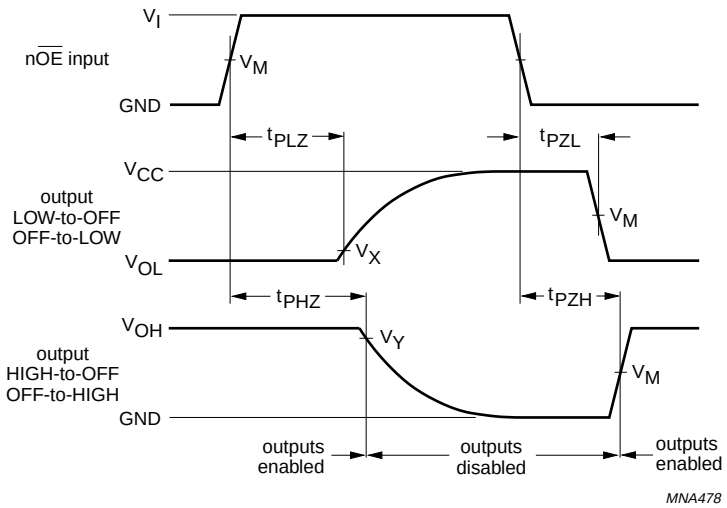
1. All typical values are measured at T_{amb} = 25 °C.
2. Value is measured at V_{CC} = 3.3 V.

AC WAVEFORMS



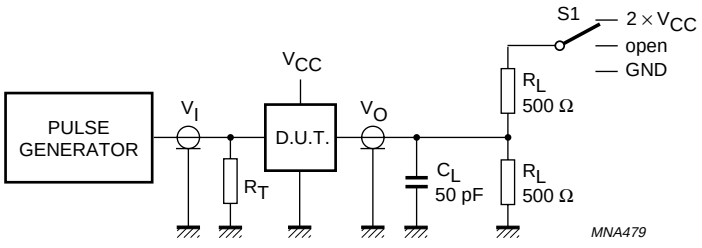
V_M = 1.5 V at $V_{CC} \geq 2.7$ V or
$V_M = 0.5 \times V_{CC}$ at $V_{CC} < 2.7$ V.
V_{OL} and V_{OH} are typical output voltage drop that occur with the output load.

Fig.4 Input nAn to output nYn propagation delay times.



V_M = 1.5 V at V ≥ 2.7 V or
$V_M = 0.5 \times V_{CC}$ at V_{CC} < 2.7 V;
$V_X = V_{OL}$ + 0.3 V at $V_{CC} \geq$ 2.7 V or
$V_X = V_{OL}$ + 0.1 V at V_{CC} < 2.7 V;
$V_Y = V_{OH}$ − 0.3 V at $V_{CC} \geq$ 2.7 V or
$V_Y = V_{OH}$ − 0.1 V at V_{CC} < 2.7 V.
V_{OL} and V_{OH} are typical output voltage drop that occur with the output load.

Fig.5 3-state enable and disable times.



TEST	S1
t_{PLH}/t_{PHL}	open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PZH}	GND

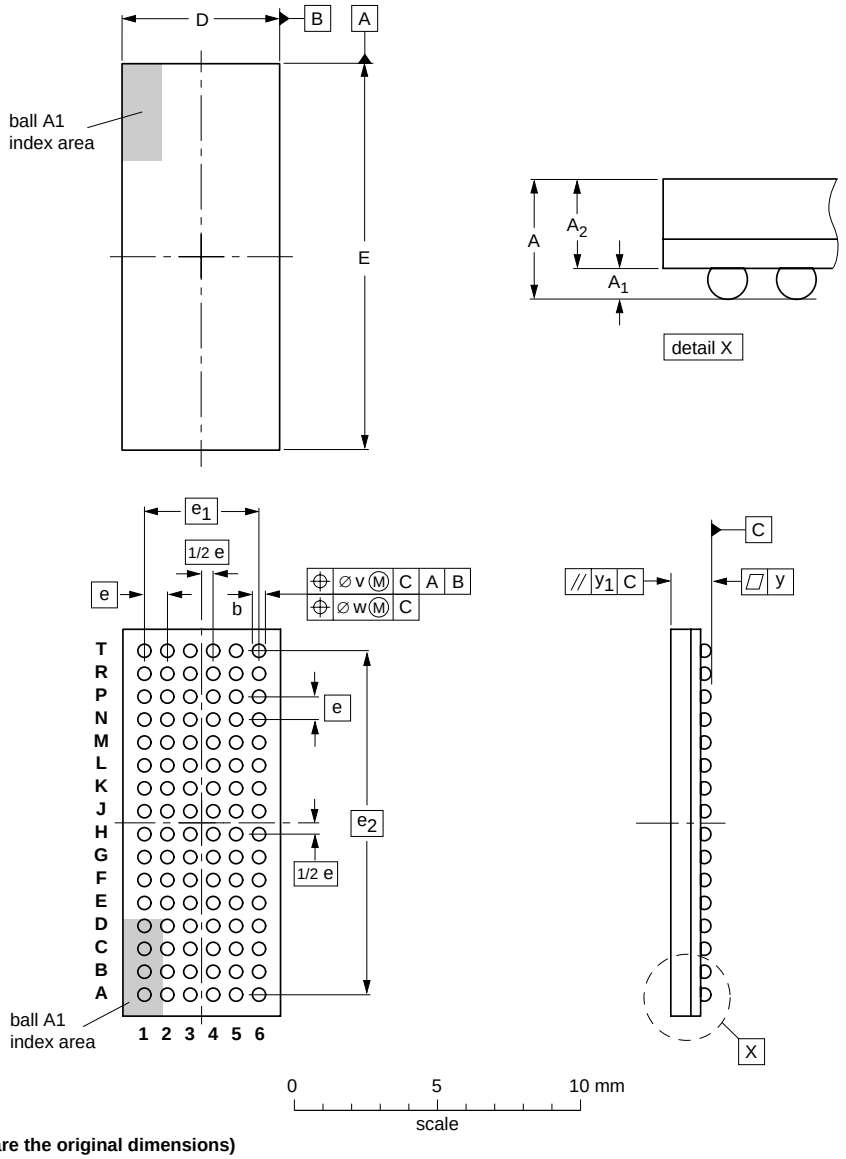
V_{CC}	V_I
< 2.7 V	V_{CC}
2.7 V to 3.6 V	2.7 V

Definitions for test circuit:
R_L = load resistor.
C_L = load capacitance including jig and probe capacitance.
R_T = termination resistance should be equal to the output impedance Z_o of the pulse generator.

Fig.6 Load circuitry for switching times.

PACKAGE OUTLINE

LFBGA96: plastic low profile fine-pitch ball grid array package; 96 balls; body 13.5 x 5.5 x 1.05 mm SOT536-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	b	D	E	e	e_1	e_2	v	w	y	y_1
mm	1.5	0.41 0.31	1.2 0.9	0.51 0.41	5.6 5.4	13.6 13.4	0.8	4	12	0.15	0.1	0.1	0.2

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT536-1						~~00-03-04~~ 03-02-05

DATA SHEET STATUS

LEVEL	DATA SHEET STATUS(1)	PRODUCT STATUS(2)(3)	DEFINITION
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Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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